AMENDMENTS TO THE CLAIMS

Claims 15-18 and 24-46 are pending. Please amend claims 15, 24, 28, 32, 37, and 42 as follows, without acquiescence or prejudice to pursue the original claims in a related application. No new matter has been added. A complete listing of the current pending claims is provided below and supersedes all previous claims listing(s).

1-14. (Cancelled)

15. (Currently Amended) An apparatus comprising:

means for dividing p pins of an integrated circuit into n groups;

means for logically associating the pins of each group through an ExOR matrix; and

means for driving a plurality of scan chains in the integrated circuit with the logically associated pins, wherein the plurality of scan chains are driven by ExORing the pins from the n groups, and the ExOR matrix is configured such that the number of pins logically associated through the ExOR matrix is less than the number of scan chains coupled to the ExOR matrix.

16. (Original) The apparatus of claim 15, wherein said means for logically associating the pins further comprises:

means for generating (p/n)^n logical associations, where p is the number of pins, and n is the number of groups of pins.

17. (Original) The apparatus of claim 15, wherein the number of scan chains is equal to the number of logical associations.

18. (Original) The apparatus of claim 15, wherein the ExOR matrix has n dimensions.

19-23. (Cancelled)

24. (Currently Amended) ~~An article of manufacture comprising:~~

~~a~~ computer readable medium having stored thereon ~~storing~~ a computer program which, when executed by a processor, causes the execution of a process, the medium comprising:

code for dividing p pins of an integrated circuit into n groups;

code for logically associating the pins of each group through an ExOR matrix; ~~and~~

code for driving a plurality of scan chains in the integrated circuit with the logically associated pins, wherein the plurality of scan chains are driven by ExORing the pins from the n

groups, and the ExOr matrix is configured such that the number of pins logically associated through the ExOR matrix is less than the number of scan chains coupled to the ExOR matrix; and

code for storing a result of a logical operation performed by the ExOR matrix.

25. (Original) The medium of claim 24, wherein said code for logically associating the pins further comprises:

code for generating (p/n)^n logical associations, where p is the number of pins, and n is the number of groups of pins.

26. (Original) The medium of claim 24, wherein the number of scan chains is equal to the number of logical associations.

27. (Original) The medium of claim 24, wherein the ExOR matrix has n dimensions.

28. (Currently Amended) A method comprising:

dividing p pins of an integrated circuit into n groups;

logically associating the pins of each group through an ExOR matrix; and

driving a plurality of scan chains in the integrated circuit with the logically associated pins, wherein the plurality of scan chains are driven by ExORing the pins from the n groups, and the ExOR matrix is configured such that the number of pins logically associated through the ExOR matrix is less than the number of scan chains coupled to the ExOR matrix.

29. (Previously Presented) The method of claim 28, wherein said logically associating the pins further comprises:

generating (p/n)^n logical associations, where p is the number of pins, and n is the number of groups of pins.

30. (Previously Presented) The method of claim 28, wherein the number of scan chains is equal to the number of logical associations.

31. (Previously Presented) The method of claim 28, wherein the ExOR matrix has n dimensions.

32. (Currently Amended) A method comprising:

dividing pins of an integrated circuit into a first group and a second group;

logically associating each pin of the first group to each pin of the second group; and

generating a scan chain in the integrated circuit for each logical association of pins, wherein each ~~the~~ scan chain is driven by logically associating the pins from the two groups, and the pins and scan chains are configured such that the number of pins is less than the number of scan chains.

33. (Previously Presented) The method of claim 32, further comprising:

driving the scan chains with the logical association of pins.

34. (Previously Presented) The method of claim 33, wherein the first group has n number of pins, the second group has m number of pins, and the logical association of pins drives n*m scan chains.

35. (Previously Presented) The method of claim 32, wherein logically associating comprises:

performing an exclusive OR operation.

36. (Previously Presented) The method of claim 35, wherein generating the scan chains comprises:

C[i][j] <= a[i] ExOR b[j]

where a[i] is a pin in the first group; b[j] is a pin in the second group; i = 1 to n; and j = 1 to m.

37. (Currently Amended) An apparatus comprising:

means for dividing pins of an integrated circuit into a first group and a second group;

means for logically associating each pin of the first group to each pin of the second group; and

means for generating a scan chain in the integrated circuit for each logical association of pins, wherein the scan chain is driven by logically associating the pins from the two groups, and the pins and scan chains are configured such that the number of pins is less than the number of scan chains.

38. (Previously Presented) The apparatus of claim 37, further comprising:

means for driving the scan chains with the logical association of pins.

39. (Previously Presented) The apparatus of claim 38, wherein the first group has n number of pins, the second group has m number of pins, and the logical association of pins drives n*m scan chains.

40. (Previously Presented) The apparatus of claim 37, wherein said means for logically associating comprises:

means for performing an exclusive OR operation.

41. (Previously Presented) The apparatus of claim 40, wherein said means for generating the scan chains comprises:

means for determining C[i][j] <= a[i] ExOR b[j]

where a[i] is a pin in the first group; b[j] is a pin in the second group; i = 1 to n; and j = 1 to m.

42. (Currently Amended) ~~An article of manufacture comprising:~~

~~a~~ computer readable medium having stored thereon ~~storing~~ a computer program which, when executed by a processor, causes the execution of a process, the medium comprising:

code for dividing pins of an integrated circuit into a first group and a second group;

code for logically associating each pin of the first group to each pin of the second group;

code for generating a scan chain in the integrated circuit for each logical association of pins, wherein the scan chain is driven by logically associating the pins from the two groups, and the pins and scan chains are configured such that the number of pins is less than the number of scan chains; and

code for storing a result of a logical operation performed by the logical association.

43. (Previously Presented) The medium of claim 42, wherein the program further comprises:

code for driving the scan chains with the logical association of pins.

44. (Previously Presented) The medium of claim 43, wherein the first group has n number of pins, the second group has m number of pins, and the logical association of pins drives n*m scan chains.

45. (Previously Presented) The medium of claim 42, wherein said code for logically associating comprises:

code for performing an exclusive OR operation.

46. (Previously Presented) The medium of claim 45, wherein said code for generating the scan chains comprises:

code for determining C[i][j] <= a[i] ExOR b[j]

where a[i] is a pin in the first group; b[j] is a pin in the second group; i = 1 to n; and j = 1 to m.